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CHARACTERIZATION OF A CMOS SENSING CORE FOR ULTRA-MINIATURE WIRELESS IMPLANTABLE TEMPERATURE SENSORS WITH APPLICATION TO CRYOMEDICINE

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Abstract

In effort to improve thermal control in minimally invasive cryosurgery, the concept of a miniature, wireless, implantable sensing unit has been developed recently. The sensing unit integrates a wireless power delivery mechanism, wireless communication means, and a sensing core—the subject matter of the current study. The current study presents a CMOS ultra-miniature PTAT temperature sensing core and focuses on design principles, fabrication of a proof-of-concept, and characterization in a cryogenic environment. For this purpose, a 100μm × 400μm sensing core prototype has been fabricated using a 130nm CMOS process. The senor has shown to operate between −180°C and room temperature, to consume power of less than 1μW, and to have an uncertainty range of 1.4°C and non-linearity of 1.1%. Results of this study suggest that the sensing core is ready to be integrated in the sensing unit, where system integration is the subject matter of a parallel effort.

Keywords

Temperature Sensor; Miniature; Ultra Low-Power; Implant; All-CMOS; Cryomedicine; Cryosurgery

INTRODUCTION

Cryosurgery is the controlled destruction of undesired tissues by freezing, known as an invasive surgical technique since the early 1960s [1]. Cryosurgery has been experimented and practiced as a minimally invasive procedure since the middle of the 1990s, in

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conjunction with concurrent developments in medical imaging such as ultrasound [2], CT [3,4], and MRI [5,6]. Medical imaging has been successfully used to monitor the growth of the frozen region during the procedure as an indicator of cryosurgery success.

While criteria for cryosurgery success are well established in the cryobiology literature [7], most frequently correlated with the temperature field and the local cooling and rewarming rates, effective means to measure the temperature distribution in the treated area in real time represent an unmet need. At best, current practices rely on temperature sensors embedded at the tip of the cryoprobes and possibly one or two additional sensors strategically placed at the tip of long hypodermic needles. These sensors are cumbersome to operate and do not provide sufficient data to reconstruct the local temperature distribution. Hence, minimally invasive cryoprocedures relying solely on medical imaging represent common practice to date.

Ultrasound-monitored prostate cryosurgery was the first minimally invasive procedure to pass from the experimental stage to routine practice, yet the quality of the image in the unfrozen region and shadowing effects by the frozen region [8] represent major challenges in correlating the frozen region with the shape of the target area [9]. To prevent one of the most severe complications of the procedure—cryoinjury to the rectum—a single temperature sensor at the tip of a hypodermic needle is often placed between the prostate and the rectal wall. The application of a single temperature sensor, combined with the associated uncertainties in measurements [10], is often ineffective in preventing cryoinjury to the surrounding tissues.

In effort to improve thermal control in minimally invasive cryosurgery, the concept of miniature, wireless, implantable sensors for cryogenic temperatures has been developed recently [11]. Here, an integrated sensing unit is powered by magnetic induction, communicated with wirelessly, where the temperature is measured by a sensing core—the subject matter of the current report. The integrated sensing unit is expected to operate in the entire temperature range applicable to cryosurgery of −196°C to 37°C, while consuming less than 1μW of power, which is deemed consistent with the potential to deliver power by induction. The temperature measurements are then used to reconstruct the temperature field by solving the inverse thermal problem in close-to-real time [12]. While several integrated temperature sensors have been presented in the literature [13,14,15], they do not meet the above specifications and, hence, they do not represent viable alternatives for the sensing core presented in the current study.

As a part of an ongoing effort to develop miniature implantable temperature sensors with application to cryosurgery, the current study presents an all-CMOS temperature sensing core. This study focuses on design principles, fabrication of a proof-of-concept, and its characterization in a cryogenic environment.

PRINCIPLES OF SENSOR DESIGN AND IMPLEMENTATION

A schematic illustration of the proposed design for proportional-to-absolute-temperature (PTAT) sensor is displayed in Fig. 1, where Q_1 and Q_2 are nominally identical PNP bipolar junction transistors (BJTs), implemented using the substrate PNP structure inherent to

standard CMOS technologies. The operational amplifier (op-amp; A_{DM} in Fig. 1) forces the drain voltages of the metal-oxide semiconductor field-effect transistors (MOSFET) M_1 and M_2 to equate by means of negative feedback. By selecting the width of M_2 to equal n_0 times the width of M_1, the drain current of M_2 becomes n_0 times the drain current of M_1 (annotated I_0). It follows that the difference between the emitter-base voltages V_{EB1} and V_{EB2} of transistors Q_1 and Q_2, respectively, (Fig. 1) can be approximated as [16]:

$$\Delta V_{EB}=V_{EB2}-V_{EB1}=\Phi_T \quad ln\left(\frac{n_0 I_0}{I_S}\frac{I_S}{I_0}\right)=\Phi_T \quad ln\,(n_0) \quad \text{where} \quad \Phi_T=\frac{kT}{q} \quad (1)$$

where I_S is the reverse saturation current of the BJT's, Φ_T is the thermal voltage, k is the Boltzmann constant (1.381×10^{-23} J/K), q is the electronic charge (1.6×10^{-19}C), and T is the absolute temperature. Note that the current I_0 has a PTAT characteristic since it represents the ratio of ΔV_{EB} to R_B. The natural logarithm of the current ratio n_0 in Eq. (1) determines the constant of proportionality between the sensor's output voltage, ΔV_{EB}, and the absolute temperature.

The primary advantage in a PTAT-based temperature sensor is that n_0 is nominally equal to the ratio of lithographically defined transistor widths, which is closely controlled in CMOS fabrication. While Eq. (1) provides insight into the operational principles of the temperature sensor, the model needs to be expanded to account for non-idealities which arise in a practical implementation, as described below.

Nonlinearity in the Proposed Design

The formulation for the output voltage, Eq. (1), is now expanded to account for non-linearities that affect the certainty in temperature sensing in the proposed design, including:

- **N1** Mismatch in geometrical and process parameters between nominally identical transistors Q_1 and Q_2.
- **N2** Mismatch in extrinsic base resistance and emitter resistance between Q_1 and Q_2.
- **N3** Mismatches in geometrical and process parameters between M_1 and M_2.
- **N4** Finite low-frequency gain (i.e., DC gain) and systematic and random offset voltages of the operational amplifier. The systematic offset voltage results from the design of the differential to single-ended stage of the operational amplifier. The random offset results from random mismatches between the two nominally symmetric branches of the differential stages of the operational amplifier.

With reference to Fig. 2, by expressing all mismatched parameters in terms of their nominal (average) value and the corresponding deviation from the nominal value (the deviation is displayed in terms of uncertainty), while employing basic circuit analysis techniques, the emitter-base voltage difference can be expressed as:

$$\Delta V_{EB} \approx \Phi_T \quad ln \quad n+\Phi_T \quad ln\left(1+\frac{\Delta I_S}{I_S}\right)\left(1+\frac{\Delta\beta}{\beta\,(\beta+1)}\right)+(n-1)\,I_0 R_{EFF}+(n+1)\,\frac{I_0\Delta R_{EFF}}{2} \quad (2)$$

where n is the actual emitter current ratio I_{E2}/I_{E1}, β is the current gain factor of the PNP transistor, equal to the ratio of its collector to base currents, and:

$$R_{EFF}=R_E+\frac{R_B}{\beta+1} \quad ; \quad \Delta R_{EFF}=\Delta R_E+\frac{\Delta R_B}{\beta+1}-\frac{\Delta\beta}{(\beta+1)^2} \quad (3)$$

where R_B and R_E are the nominally identical base and emitter resistances of both transistors Q_1 and Q_2, while ΔR_B and ΔR_E are the differences between the corresponding resistor values for the two transistors.

Equation (2) can be further simplified by assuming that the uncertainties are small compared to the corresponding nominal values, and applying the approximation $\ln(1 + x) \approx x$:

$$\Delta V_{EB} \approx \Phi_T \quad ln \quad n+\Phi_T\left(\frac{\Delta I_S}{I_S}+\frac{\Delta\beta}{\beta\,(\beta+1)}\right)+(n-1)\,I_0R_{EFF}+(n+1)\,\frac{I_0\Delta R_{EFF}}{2} \quad (4)$$

The first term on the right-hand side in Eq. (4) is similar to the ideal case presented in Eq. (1), with the exception that the current ratio n is no longer equal to a nominal lithographically defined value. The second term represents the mismatch between the saturation current and current gain factor of the two otherwise nominally identical transistors Q_1 and Q_2. However, an order-of-magnitude analysis of this second term suggests that it would contribute less than 0.01°C to the uncertainty in temperature and therefore may be neglected. The remaining terms in Eq. (4) quantify the effects of the extrinsic resistance, R_{EFF}, and the mismatch between its transistors values Q_1 and Q_2 (ΔR_{EFF}).

Effects N3 and N4 typically cause the current ratio n to deviate from its nominal value n_0. In the proposed design, the transistors M_1 and M_2 are biased in the sub-threshold region of operation ($V_{SG}<|V_{TH}|$), in contrast to typical designs that operate in strong inversion ($V_{SG}>|V_{TH}|$). Based on a simplified form of the BSIM2 level-5 MOSFET circuit simulation model [17], the currents in M_1 and M_2 may be expressed as:

$$I_i=\beta_{P_i}\,(\eta_i-1)\,\Phi_T^2 \quad exp\left(\frac{V_{SG}-V_{THi}+\lambda_1V_{SDi}}{\eta_i\Phi_T}\right)\left[1-exp\left(\frac{-V_{SDi}}{\Phi_T}\right)\right] \quad (5)$$

where η_i is the sub-threshold swing parameter, V_{THi} is the threshold voltage, λ_1 is the drain-induced barrier lowering coefficient, V_{SDi} is the source-drain voltage, V_{SG} is the source-gate voltage, i represents either transistor M_1 or M_2, and the following parameter is defined for brevity:

$$\beta_{Pi}=\mu_PC_{OX}(W/L)_i \quad (6)$$

where μ_P is the hole mobility in cm^2/Vs, C_{ox} is the oxide capacitance per unit area in F/m^2, and $(W/L)_i$ is the width to length ratio of the transistors i.

An expression for the deviation of current ratio n from its nominal value n_0 may now be expressed in terms of:

$$\Delta_n=\frac{\Delta\beta_P}{\beta_P}-\frac{\Delta V_{TH}}{\eta\Phi_T}+\frac{\lambda\Delta V_{SD}}{\eta\Phi_T}+\frac{\Delta\eta}{\eta}\left(\frac{\eta}{\eta-1}-\frac{V_{SG}-V_{TH}}{\eta\Phi_T}-\frac{\lambda V_{SD,CM}}{\eta\Phi_T}\right)-\frac{\Delta\lambda V_{SD,CM}}{\eta\Phi_T} \quad (7)$$

where $n\approx n_0(1+\Delta n)$, β_P is the average of β_{P2}/n_0 and β_{P1}, $\Delta\beta_P$ is the difference between β_{P2}/n_0 and β_{P1}, $V_{SD,CM}$ is the average (common-mode) of V_{SD2} and V_{SD1}, and ΔV_{SD} is the difference between V_{SD2} and V_{SD1}. The voltage term ΔV_{SD} in Eq. (7) is a function of the op-amp's finite differential-mode dc gain, A_{DM}, and the input-referred offset voltage, V_{OS}. For this purpose, the op-amp's output voltage is written as:

$$V_0=A_{DM}\left[(V_+-V_-)+V_{OS}\right] \quad (8)$$

where the op-amp's positive and negative input terminal voltages are equal to the difference between supply voltage, V_{DD}, and the drain-to-source voltages V_{SD2} and V_{SD1}, respectively (i.e., $V_+=V_{DD}-V_{SD2}$ and $V_-=V_{DD}-V_{SD1}$). The difference between V_{DD} and V_O, is equal to the source-gate voltages V_{SG} of M_1 and M_2. It follows that the voltage difference, ΔV_{SD}, can be expressed as:

$$\Delta V_{SD}=\frac{V_{DD}-V_{SG}}{A_{DM}}-V_{OS} \quad (9)$$

An expression for Δn may now be obtained by substituting Eq.(9) in Eq. (7). Finally, the sensor's output voltage ΔV_{EB} can be expressed as:

$$\Delta V_{EB}\approx\Phi_T \quad ln \quad n_0+\Phi_T\Delta n+\Phi_T\left(\frac{\Delta I_S}{I_S}+\frac{\Delta\beta}{\beta(\beta+1)}\right)+(n-1)I_0R_{EFF}+(n+1)\frac{I_0\Delta R_{EFF}}{2} \quad (10)$$

Sensor Calibration

Due to the temperature dependencies of the various terms in Eq. (10), ΔV_{EB} may become non-linearly dependent on temperature and can be generally expressed as:

$$\Delta V_{EB}=C_{T0}+C_{T1}T+g(T) \quad (11)$$

where C_{T0} and C_{T1} are constants and g denotes a function. The temperature as a function of voltage ΔV_{EB} represents the sensor reading, and can be expressed as:

$$T=C_{V0}+C_{V1}\Delta V_{EB}+f(\Delta V_{EB}) \quad (12)$$

where C_{V0} and C_{V1} are constants, and f is another function.

In the ideal case, where ΔV_{EB} is defined by Eq. (1), C_{T0} and $f(T)$ become zero and the right hand side term of Eq. (11) simply equals C_{T1}. In this case, $f(\Delta V_{EB})$ in Eq. (12) is also zero and C_{V0} and C_{V1} can be found by a two-point calibration technique:

$$T=C_{V0}+C_{V1}\Delta V_{EB} \quad ; \quad C_{V1}=\frac{\Delta V_{EB}(T_2)-\Delta V_{EB}(T_1)}{T_2-T_1} \quad ; \quad C_{V0}=(1+C_{V1})T_1 \quad (13)$$

where T_1 and T_2 are calibration temperatures at selected voltages.

In order to establish the potential magnitude of the non-linear effects N1-N4 on the calibrated curve, the circuit operation was simulated using the Specter simulator using component models made available by the CMOS foundry. Since the cryogenic temperature range is outside of the nominal model ranges, simulation results were based on extrapolation of the circuit model parameters. The resulting uncertainties, representing the differences between the calibrated values and the estimated temperatures when non-linear effects are considered, are listed in Table 1.

Methods such as dynamic element matching and chopping have previously been used to reduce uncertainties in temperature measurements resulting from similar mismatches to those listed in N1-N4, as listed in Table 2. For example, dynamic element matching (DEM) [14] can be used to reduce the effects of $\Delta\eta$, $\Delta\beta_P$, ΔV_{TH}, and $\Delta\lambda$, while chopping within the op-amp [15] and the PNP BJT's can be incorporated to mitigate the effects of ΔR_E, ΔR_B, ΔI_S, $\Delta\beta$, and V_{OS}. By using such methods, the measurement uncertainty can be decreased at the expense of increased power consumption. Using dynamic methods requires clock synthesis, which requires an oscillator—either free running or locked to a wirelessly received signal. The power required for switching and clock generation in DEM and chopping is relatively small (of the order of 10 nW). However, the PTAT core circuitry (i.e., the core transistors and the op-amp) needs to have a sufficient gain-bandwidth product to accommodate the switching [18]. When applying feedback circuit techniques to ease the gain-bandwidth requirements of the amplifier (see [19] for example), the power consumption of the circuit is of the order of 10 μW, which makes the design of a sub-microwatt sensor impossible. For these reasons, techniques to reduce the dynamic temperature uncertainties are not applicable in the current study.

EXPERIMENTAL SETUP

Figure 3 displays the designed sensor fabricated using a standard 130nm CMOS process in a commercial foundry. The area occupied by the sensing core is 100μm × 400μm, which makes it an excellent candidate to be incorporated into an implantable sensor, and can be delivered into the body by means of a hypodermic needle. In its normal operational mode, the circuit is entirely self-biased, where the op-amp bias current is generated internally and is PTAT. The circuit can also be operated in a test mode using an external current source to provide the op-amp bias current, a case in which the bias current can be designed to have any desired dependency on temperature. Since only the sensing core of the wireless, implantable, temperature sensing device is under investigation in the current study, while wireless telemetry is the subject matter of a parallel study, the sensing core was hosted in a standard IC package. A custom printed circuit board (PCB) has been fabricated to characterize the chip. The sensor outputs, V_{EB1} and V_{EB2}, were buffered with amplifiers external to the chip (on the same PCB), in order to drive the loads of the measurement instruments. The sensor outputs were measured at a sampling rate of 0.2 Hz using a high accuracy Keithley 2400 Source Measure Unit.

Characterization of the sensor at cryogenic temperatures was performed in a controlled-rate cooler (Kryo 10-16 chamber and Kryo 10-20 controller, Planer Ltd., UK), as illustrated in Fig. 4. Cooling in the Kryo 10-16 chamber is achieved by circulating a mixture of nitrogen

vapors and air at high velocity (up to 15 m/s). In order to protect the sensing core and the PCB board, a cryogenic holding stage was designed and constructed, as illustrated in Fig. 4(b).

The temperature sensor was benchmarked against temperature measurements obtained with a T-type thermocouple, placed on the PCB next to the chip, in continuous data logging mode (OMB DAQ-56, Omega Engineering, Inc.). Data acquisition for the thermocouple and the new sensor was done concurrently and independently.

RESULTS AND DISCUSSION

Figure 5 displays results obtained with two specimens of the sensing core at a sampling rate of 0.2 Hz; both specimens were fabricated on the same wafer. The thermal protocol included a sequence of cooling ramps, separated apart by constant-temperature holding periods, which were long enough to let the system reach steady state at each temperature level. Each temperature data point in Fig. 5 represents an average and standard deviation of 30 consecutive readings at steady state in order to reduce uncertainties in measurements.

Foundry models for sensor design cover the temperature range of −55°C to +125°C, while cryosurgery applications may call for temperature sensing down to the liquid nitrogen boiling temperature of −196°C. In the absence of comparable data at the sensor design stage, simulations were performed with extrapolated values on available models, which predicted system failure at temperature lower than −150°C. Experimental results in the current study demonstrated system failure at higher temperatures of −100°C and −140°C for Chips 1 and 2 in a self-PTAT self-bias mode, respectively (Fig. 5). This failure occurs when the op-amp gain drops drastically with temperature, preventing the op-amp from maintaining negative feedback in the loop. In order to overcome this problem in later experiments, external bias was used with the op-amp's to ensure negative feedback loop over the entire temperature range achievable with the Kryo 10-16 cooling chamber, down to −180°C. In liquid-nitrogen based cryosurgery, the −180°C isotherm is at a very close proximity to the cryoprobe, which is held at −196°C, and the temperature can be easily interpolated within this space. In Joule-Thomson based cryosurgery, the −180°C boundary value is lower by about 35°C from the minimum achievable temperature at the cryoprobe.

Experimental results demonstrate a very high linearity of the sensor output with temperature in a range of −180°C and −20°C, with maximum observed nonlinearity of 2°C of full scale (1.1%). While potential sources for nonlinearity in the proposed design have been discussed above, no nonlinearity mitigation techniques were deemed necessary for cryosurgery applications. Reducing nonlinear effects would unnecessarily increase the power overhead associated with the corresponding mitigation mechanisms.

The uncertainty range, defined by twice the standard deviation (2σ) at steady state, was found to vary with temperature, but to not exceeding 1.4°C in all studied cases. While this range is deemed adequate for cryosurgery application, it is higher than that predicted in Table 1, based on computerized design tools. This difference can be partly attributed to: (1) temperature variations inside the cooling chamber, were its temperature is controlled by

periodic ejection of liquid nitrogen into a highly turbulent air stream; (2) uncertainty in reference temperature, where the reference thermocouple is specified to have an uncertainty range of 1.4°C at −100°C; and, (3) electronic noises in off-chip buffer, cables, and multi-meter, which may be eliminated in a wireless implementation.

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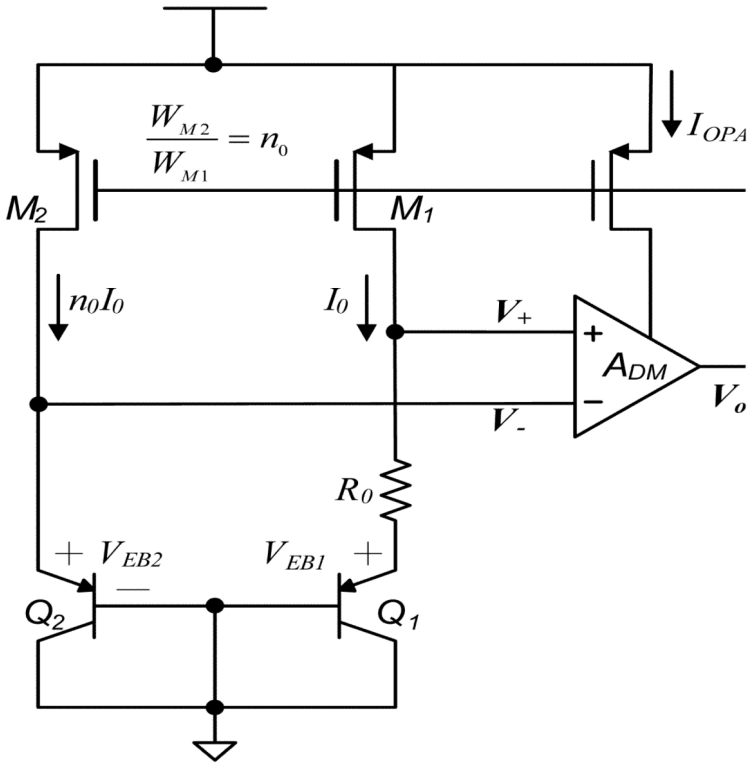
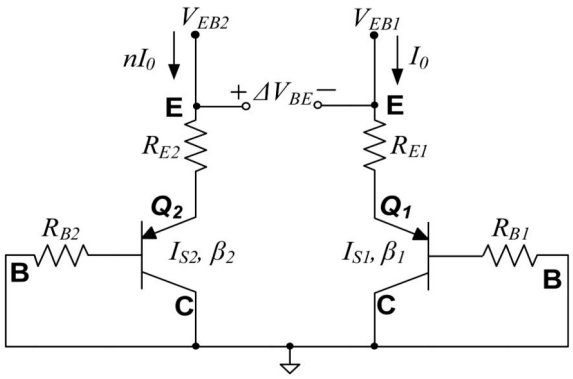


Figure 1.
Schematic illustration of the proposed proportional-to-absolute-temperature (PTAT) sensing core



$$R_{E1} = R_E - \frac{\Delta R_E}{2} \quad R_{E2} = R_E + \frac{\Delta R_E}{2}$$

$$R_{B1} = R_B - \frac{\Delta R_B}{2} \quad R_{B2} = R_B + \frac{\Delta R_B}{2}$$

$$\beta_1 = \beta - \frac{\Delta\beta}{2} \quad I_{S1} = I_S - \frac{\Delta I_S}{2}$$

$$\beta_2 = \beta + \frac{\Delta\beta}{2} \quad I_{S2} = I_S + \frac{\Delta I_S}{2}$$

$$R_{EFF1} = R_{EFF} - \frac{\Delta R_{EFF}}{2}$$

$$R_{EFF2} = R_{EFF} + \frac{\Delta R_{EFF}}{2}$$

Figure 2.

Schematic illustration of the circuit model of the BJT's in the PTAT including non-ideal parasitic resistances R_{B1}, R_{B2}, R_{E1} and R_{E2}.

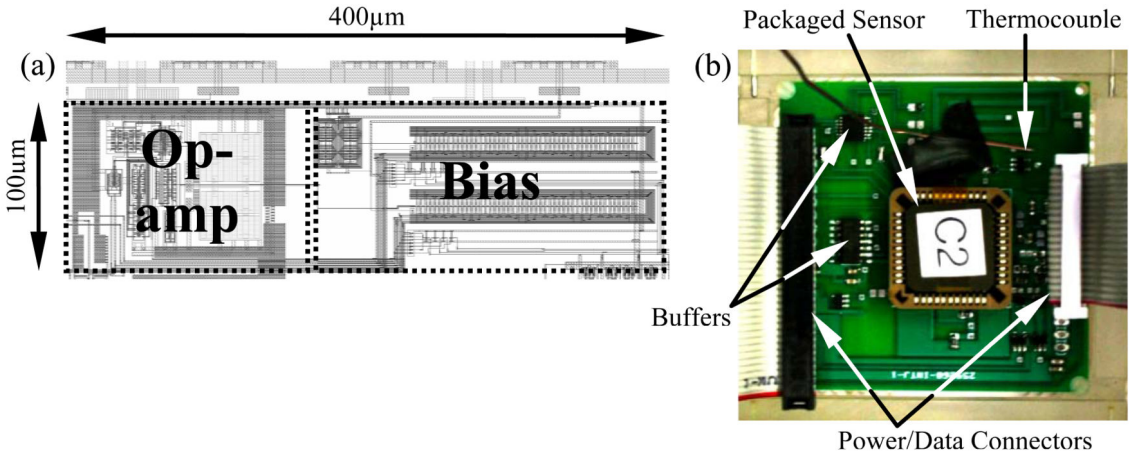


Figure 3.
Photograph of the fabricated sensor chip (a) and the packaged chip mounted on PCB (b)

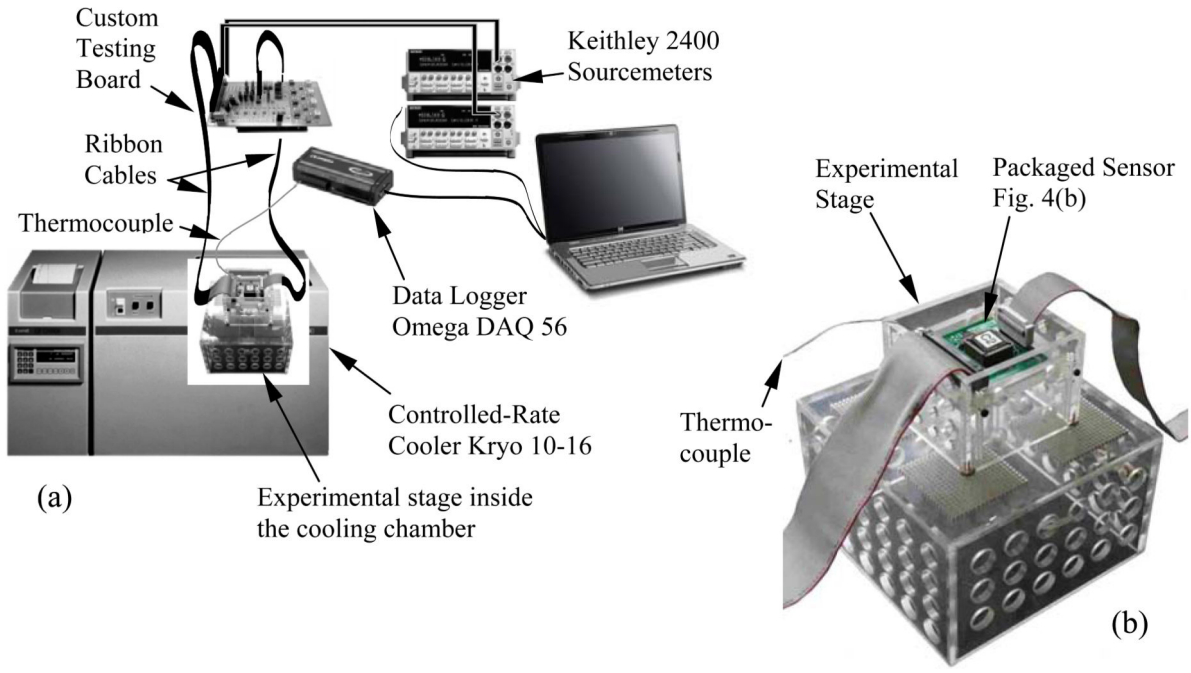


Figure 4.
Experimental setup: (a) a schematic illustration of the system, and (b) a photograph of the experimental stage

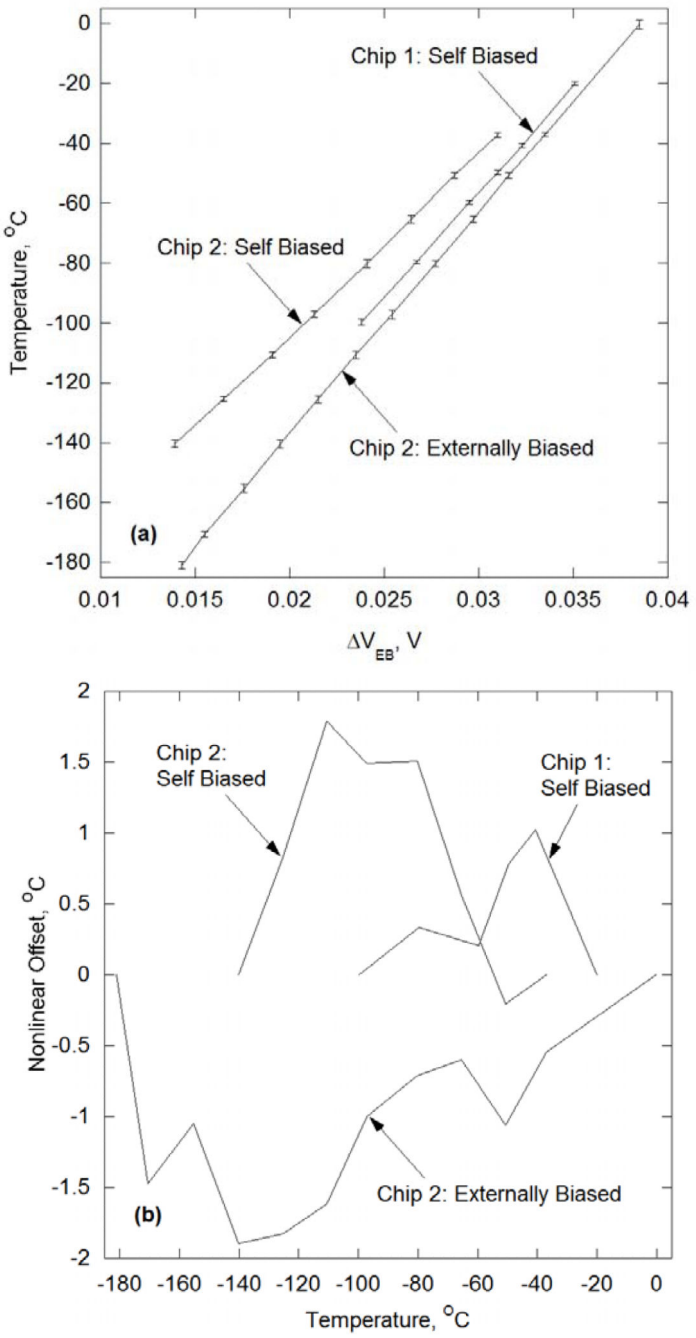


Figure 5.

Results obtained from three representative chips in a self-biased mode (#1 and #2) and an externally biased mode (#2): (a) temperature data as a function of voltage output, and (b) average nonlinear offset, calculated as the temperature difference between the experimental data shown in Fig. (a) and a linear curve connecting the boundary temperature values for each dataset.

Table 1

Theoretical analysis of the contribution of sensor components to the overall uncertainty of the proposed sensor, based on foundry-provided CMOS computation models; the overall uncertainty represents the square root of the sum of the square individual uncertainties.

Parameter	Typical	Variation	ΔT
R_B	100Ω	negligible	-
R_E	200mΩ	negligible	-
β	1.7 A/A	0.03 A/A	0.05°C
$\Delta\beta$	0.04 A/A	0.01 A/A	
V_{DD}-V_{SG}	1.075V	0.16V	0.70°C
V_{OS}	+/−10mV	1.5mV	
$(V_{DD}$-$V_{SG})/A0$	10mV	1.5mV	
V_{TH}	−230mV	2.5mV	0.20°C
ΔV_{TH}	1mV	2mV	
η	1.1	negligible	-
λ	0.01/V	negligible	-
Overall Uncertainty			0.73°C

Table 2

Performance comparison of the current design with literature data

	Current study	Sebastiano et al. [14]	Aita et al. [15]	Shih et al. [13]
Modulation	Analog*	Sync. ΔΣ	Sync. ΔΣ	Frequency
Uncertainty	1°c**	0.2°C	0.1°C	0.4°C
Range	−180°C to 0°C	−70°C to 125°C	−70°C to 130°C	25°C to 45°C
Supply	1.2-1.3V	1.2-1.3V	2.2-5.5V	1.2V
Power	1μW	10μW	63μW	2.3μW
Process	130nm	65nm	0.7μm	130nm
Area	0.13mm^2	0.1mm^2	4.5mm^2	0.7mm^2

* The current setup doesn't include a modulation scheme which exists in other systems but consumes additional power

** Not calibrated for external noise and nonlinearity