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FABRICS II: A STATISTICAL SIMULATOR
OF THE IC FABRICA PROCESS

by

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A STATISTICAL SIMULATOR OF THE IC FABRICATION PROCESS*
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Abstract
This paper describes a Statistical Process Simulator FABRICS II developed at Carnegie-Mellon University, as part of a design verification/optimization package. In this package the process simulator is used with a multilevel circuit simulator, SAMSON pi to simulate KT's at the process, circuit and logic levels. Possible applications of FABRICS include verification and optimization of nominal process and circuit design, yield failure analysis. The current implementation of FABRICS II is briefly described and an example illustrating the application of FABRICS II to process optimization is presented.

Introduction
Most of the VLSI design systems which are being developed at present employ a structured (hierarchical) design methodology (J). A VLSI system is partitioned into modules with well defined interfaces. The syntheses proceeds in a top-down manner from the high level behavioral description to the IC mask level. Due to the complexity of VLSI, the design cycle must contain a design verification feedback loop. Verification consists of checking whether the implementation meets the specifications at various levels such as functional logic or layout levels, top-down automated design systems (e.g. silicon compiler) several verification tools (e.g. fault extraction, logic simulation, design rule checking) may be impractical because the system produces correct designs. However, there is a need for IC performance evaluation prior to IC manufacturing. Computer simulators is the most powerful and widely used technique for performance verification. For example a circuit simulator, SPICE is used to verify a circuit design. The accuracy of such a performance evaluation strongly depends on the accuracy of the device model parameters used in the simulation.

Generally, the set of model parameters present in circuit simulators is not valid for a particular fabrication process, so these parameters have to be extracted from measurements made on actual manufactured devices. The extraction of model parameters is difficult because they are not independent. Hence, it may be that the extracted values are significantly different from the real ones.

An alternative method of determining device parameters is to use a Process Simulator which contains physical models of fabrication steps and device models. Such a simulator may be tuned to a particular process by means of a few typical in-process measurements, and would then generate full sets of model parameters which are in good agreement with data extracted from measurements.

Due to unavoidable fluctuations which are inherent in the IC fabrication process, device parameters, and consequently IC performances, are subject to variations. Ideally an IC should be designed in such a way that variations in its performances, due to the fluctuations which occur in a normal manufacturing process, are within allowable tolerances. Traditional IC designers performed worst case analysis by varying device parameters. However, since this approach did not take into account the dependencies among these parameters, the resulting designs were often too conservative. Moreover, adjustments in design rules which were often made as a case study of the chip area which could result in the decrease in the yield value because of the catastrophic effects.

Recently an increased amount of effort has been directed toward statistical design strategies. The objective is to maximize manufacturing yield. Yield maximization is performed in terms of process and IC layout parameters. Accurate yield prediction is of crucial importance in these methods, and it is usually done by multiple evaluation of circuit performance, each evaluation being carried out with a different set of device model parameters. In order to obtain accurate results, the joint probability density function (jpdf) which describes the distribution of device model parameters must be close to that found in reality. This is especially important for monolithic KT's where the correlation coefficients between device parameters are important and agreement in means and variances is not sufficient. Data samples suitable for use in a circuit simulator, and with the correct jpdf can be generated by a Statistical Process Simulator.

In this paper we present a statistical process simulator, FABRICS II. Since the methodology behind statistical process simulation was presented in (4), here we focus our attention on the description of the structure of FABRICS II, the models which are implemented in the current version and the incorporation of FABRICS II into a design verification/optimization package for KT's.

*Th word "B mmrad m pm by die total SOOMC Promotion under Go—Wo BCSUOMMmAHalmtttuiw-cinlCa
Traditional approaches to process simulation (e.g., programs like SUPREM) employ numerical models of the fabrication steps. These models, which are described by partial differential equations (e.g., diffusion equation), are solved using numerical techniques to produce the nominal profiles of impurities in silicon. The impurity profiles are then input to device simulator* (e.g., SEDAN), in which semiconductor device models are described by a system of partial differential equations (e.g., Poisson or continuity equations). These equations are solved numerically to produce device parameters. While the accuracy of simulation results obtained from these simulators is high, these approaches become prohibitively expensive for statistical investigations, due to the complexity of the models used. Furthermore, identification of some input parameter is difficult and these programs lack a direct interface to data.

To alleviate these difficulties, we propose the use of analytical models which are solutions of the partial differential equations that describe each fabrication step, under a set of restricted or simplifying conditions, which have been found to yield reasonable results. The input to such a model would consist of process parameters, such as times and temperatures of diffusion or ion implantation, output parameters of previous modeling steps, and process disturbances. These disturbances are modeled as physical parameters, such as diffusivities of impurity atoms and misalignment between two photolithographic masks, which are random variables with probability distributions determined by tuning to a particular fabrication process. In a similar fashion, the device models are also analytic using the output of the fabrication step models, and device layout to calculate the device parameters. For a more complete description of these models, and of the tuning procedure, see [7].

It should be noted that recently analytical modeling techniques have become more popular in the area of process and device simulation. Several programs have been developed in which either analytical models or a combination of numerical and analytical models are implemented^ two-dimensional process simulator, SUPRA (8) or process and device simulator, PRIDE (9). These approaches offer a reasonable compromise between the accuracy and efficiency of simulation.

**Process Simulator**

The structure of FABI is shown in Fig. 1. The input consists of process parameters, process disturbances, and run control parameters. The following models of the fabrication steps are included:

1. **Diffusion of impurities into silicon.** Diffusion is modeled as a two-step process consisting of predeposition and drive-in. Segregation of impurity atoms between silicon and silicon dioxide is taken into account. Diffusion models for three basic dopants, i.e., phosphorus, boron, and arsenic are included.

2. **Ion implantation.** Ion implanted profiles are determined from an analytical model. Models for annealing and thermal redistribution of ion-implanted impurity atoms are also included.

3. **Thermal oxidation.** The model for oxide growth implemented in FABI takes into account the changes in the oxidation rate due to various oxidizing agents (steam, dry or wet oxygen), heavily doped substrates, and partial pressure of oxygen.

4. **Photolithography.** Statistical model for lithography operations is implemented which accounts for linewidth inaccuracy caused by misalignment, and by fluctuations inherent in optical and etching operations.

1. **Surface treatment processes** and **1x2010 deposition** are modeled statistically by the random variables representing process fluctuations (e.g., surface potential, surface recombination velocity, surface state density, specific contact resistance).

**Structure of the Simulator**

FABRICS II is the second version of the simulator described in [4]. This version is written in PASCAL and currently runs on a VAX 11/780 computer under the UNIX and VMS operating systems. New models of both fabrication steps and semiconductor devices have been added which combine** for simulation of a variety of different technologies including NMOS, CMOS, and bipolar. The structure of the simulator has been significantly changed to make it modular. It is now very easy to add a new model or modify an existing one without altering the remaining pan of the simulator. FABRICS II is composed of two major parts, called FABI and FABI each of which contains a collection of analytic models as described above.

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* run control parameters

**Disturbances**

- Set of physical parameters

**Process Parameters**

- NMOS
- BPOLAR
- CMOS

**Process Supervisor Routines**

- OMuation
- Oxidation
- Annealing

**Fabrication process routine library**

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Fig. 1. Structure of FABI
FAB] also contains models for in-line measurements such as rneck resistances and junction depths of diffusion layers, and threshold volumes of MOS transistor. A detailed description of the models implemented in a current version of the simulator can be found in [10]. Subroutines which employ the models of the fabrication steps together with the corresponding in-line measurement models are stored in a library. Each of the fabrication processes which can be simulated by FAB1 has a subroutine which contains the models of the fabrication processes stored in a library. This process supervisor, which is similar to the fabrication process flow chart, is created for each manufacturing process to be simulated. The main routine of FAB1 parses the input data and outputs the physical parameters generated in the simulator, such as parameters of impurity profiles or oxide thicknesses, to the physical factory floor.

Device Simulator FAB2 uses the physical parameters generated in FAB1, combined with the layout dimensions of semiconductor devices, to produce the device model parameters, such as the parameters of the Shichman-Hodges model of MOS transistor or the Gummel-Poon model) of a bipolar transistor. These parameters can be used in a circuit simulator to predict the performance of the circuit.

In the current implementation, there is a library of the device models. The main routine of FAB2 parses a model template and determines a list of parameters which have to be calculated. Then the model parameters are computed using functions stored in a device model library, and read to a model template to be used in the circuit simulator. The rest of the device model library contains models of semiconductor devices, such as MOS or BJT devices, which are used in SPICE and SAMSON.

Fig. 2 shows the structure of FAB2. Note that information about the dimensions of the various devices is derived from a layout description of the chip (e.g. a CIF file) using a circuit extractor [11]. This layout information is divided into two parts: device dimensions, which are used in FAB2 to calculate device parameters, and the library, which is used in FAB2 to produce R-C type elements, and used in a circuit simulator to determine delays between circuit blocks.

Applications and Examples

A design verification/optimization package consists of FABRICS II and SAMSON. The ancillary of this package is shown in Fig. 3. This package may be used as a design tool that is capable of performing a given circuit/layout at the process, circuit and logic levels. The linking of the device models and the output of one program into proper input for another program.

![Diagram](image)

Ra.3. Structure of Skmitatatkm System withPAMUCSH

FABRICS II in the statistical mode, may be used to generate data samples that can be used for yield prediction, statistical verification and yield maximization. Current work is being done on fault diagnosis of an IC manufacturing process using FABRICS II [121]. Such a simulator can also be used for process control and as a basis for a quality control system for an IC fabrication process.

To illustrate how FABRICS II can be applied to process optimization, we considered an example of a 64 bit x 64 bit dynamic RAM cell implemented in MOS technology [13]. The circuit consists of one 3-transistor memory cell, row decoder and driver, column decoder and driver, read-write buffer, and precharge circuit. The entire circuit contains 74 MOS transistors. We investigated the effect of changes of process parameters on circuit performance. In particular, the influence of gate oxidation time on power dissipation and read cycle access time was investigated. An experiment was performed in which gate oxidation time was varied, and for each value of time a sample was generated by FABRICS II. The simulator was used to a tKVtd NMOS fabrication process. The device parameters generated by FABRICS II were automatically input to SPICE for circuit simulation. The results obtained from these simulations are shown in Fig. 4 and Fig. 3. As indicated in Fig. 4, power (†ellation) monotonically decreases with increasing gate oxidation time. The effect of the increased oxide thickness is a decreased intrinsic transistor gain, which results in a decreased power dissipation. Fig. 5 indicates that the access time monotonically
increases with the increase in gate oxidation time. This is caused by the fact that the decreased intrinsic transconductance of the MOS transistor causes a drop in speed. Hence, it is possible to investigate the power-speed trade-off for various KT designs.

FABRICS II has been tuned to a standard CMOS fabrication process and the accuracy of simulation proved to be good when compared to the measurement results and SUPREM simulation. This comparison will be demonstrated in the conference presentation.

References