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We report a strong field effect observed at room temperature in epitaxially synthesized, as opposed to exfoliated, graphene. The graphene formed on the silicon face of a 4H silicon carbide substrate was photolithographically patterned into isolated active regions for the semimetal graphene-based transistors. Gold electrodes and a polymer dielectric were used in the top-gate transistors. The demonstration of a field effect mobility of 535 cm^2/Vs was attributed to the transistor geometry that maximizes conductance modulation, although the mobility is lower than observed in exfoliated graphene possibly due to grain boundaries caused by the rough morphology of the substrate surface.

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The demonstration of field effect mobility as high as 10^4 cm^2/Vs in exfoliated graphene suggests potential applications for graphene-based transistors in ultra-fast electronics.[1] The two-dimensional (2D) nature of graphene enables a reasonable modulation range of the drain current of the semimetal graphene-based field effect transistor (FET),[1] probably sufficient for certain high-frequency front-end applications. Furthermore, a band gap could be created by patterning 2D graphene into nanometers-wide strips[2] to enable semiconductor graphene nanostrip-based FETs. Although the carrier mobility will decrease with decreasing nanostrip width and increasing band gap, and will be as low as that of Si when a band gap comparable to Si is reached,[3] high-mobility, narrow-band gap semiconductor-based FETs are certainly useful for many important applications.

Nevertheless, high field effect mobility at room temperature has so far only been demonstrated in exfoliated graphene, not suitable for practical device fabrication. In order to fabricate graphene-based FETs on the wafer scale, graphene synthesized on a substrate is desirable. Previous attempt achieved only 2% modulation in the drain current at 4 K temperature with epitaxial graphene on a SiC substrate, while the Hall mobility was 15 to 1100 cm^2/Vs,[4] and was up to 2.7×10^4 cm^2/Vs in patterned small features in later work,[5] although all at cryogenic temperatures.

Here, we fabricate macroscopic-size FETs to probe the average transport property over a large area of epitaxial graphene on SiC, with minimal processing and impact to the graphene active layer. Figure 1 (a) shows the device structure, where the channel length is $L = 0.45$ mm, and the width is $W = 1.5$ mm.

Two methods have been known for decades to epitaxially synthesize graphene on solid-state substrates. Epitaxial graphene can be formed by chemical vapor deposition on the surfaces of transition metal or transition metal carbide single crystals, and the physical properties, such as phonon dispersion, of single- and few-monolayer graphene synthesized using this method have been thoroughly studied.[6] The other method exploits the thermal desorption of Si atoms from the SiC surface.[4,7]

We choose this latter method for synthesizing the graphene active material of our graphene-based FETs, for the following reasons: Firstly, SiC can be highly insulating, enabling direct FET fabrication on a graphitized SiC surface, as opposed to highly conductive metal and metal carbide substrates that require transfer of the synthesized graphene onto an insulating substrate. Secondly, SiC wafers are widely available.

Our substrates are cut from a research grade, semi-insulating 4H SiC wafer from Cree, with an epi-ready Si-terminated (0001) surface (with 0.13° unintentional mis-orientation). The quoted resistivity is $\geq 10^5$ Ωcm. The substrates were hydrogen etched (H-etched) at 1600 °C in 1 atm of H_2 (11 l/min flow rate). The samples were transferred through air into an ultra-high vacuum system where the graphitization is done at 1300 °C for 20 min, at typically 1×10^{-10} Torr pressure. This graphitization process was studied with low energy electron diffraction (LEED) and Auger electron spectroscopy (AES). In general, a $6\sqrt{3}\times6\sqrt{3}$ pattern is revealed by LEED during graphitization, indicating the start of the graphitic layer formation. Further annealing, until some of the $\sqrt{3}\times\sqrt{3}$ spots disappear and the spots associated with the carbon overlayer become brighter and predominant,[4,8,9] was used, as generally indicative of the formation of graphite multilayers.[4,8,9] The graphitization in this work was monitored with AES, which showed

a C to Si peak ratio of 9±2 following graphitization, indicating the formation of 2.5±0.5 graphene monolayers over and above a terminating SiC bilayer,[10] consistent with prior work[4] and the LEED pattern evolution described above.

Figures 1(b) and (c) show atomic force microscope (AFM) images of the H-etched surface and the graphitized surface, respectively. After H-etching flat (0001) terrace steps are formed, separated by single unit-cell-high steps of 1.0 nm.[11] This overall step-terrace structure is preserved during the graphitization, but additional surface roughness is produced by pits with depth of one or more unit cells (the formation of these pits may be influenced by the transfer of the sample through air between the H-etching and graphitization steps).

Following graphitization, 56 nm thick Au source/drain (S/D) electrodes were formed by thermally evaporating through a shadow mask. Prior to graphene patterning, electrical measurement showed high conductance between all adjacent Au S/D contacts, confirming graphitization on the insulating substrate. The graphene was then patterned into islands by oxygen plasma etching. The etch mask was AZ5214E photoresist spin coated at 4000 RPM for 30 s and soft baked at 90 °C for 60s. The photoresist was exposed at 20 mJ/cm^2. In order to use an existing shadow mask as a photo mask, the photoresist was hotplate baked at 125 °C for 60 s and flood exposed at 150 mJ/cm^2 to reverse its tone. The photoresist was then developed with 1:4 diluted AZ400K in water, followed by thorough rinsing in de-ionized water and blow drying with N_2. After etching the graphene in an oxygen plasma for 1 min, the resist was removed using MicroChem Remover PG followed by an isopropanol rinse. After graphene patterning, electrical measurement showed conductance between S/D contacts on the same graphene island but

no observable conductance between contacts on adjacent islands, confirming good isolation.

The polystyrene gate dielectric layer was spin coated at 2000 rpm for 30 s after baking the substrate at 120 °C for 10 min to dehydrate it. A10%w/w polystyrene in toluene solution pre-filtered through a 2 μm syringe filter was used. Immediately after spin coating, the substrate was first dried at 85 °C for 10 min in air, and then further baked at 120 °C for 30 min in N_2. Finally, 66 nm thick Au gate electrodes were thermally evaporated through another shadow mask. An n++ doped Si control substrate, without intentional oxide, was coated with polystyrene in the same manner for capacitance and thickness measurements.

Following an overnight bake at 120 °C in N_2, the completed FETs were characterized at room temperature in air (~20% relative humidity) and various controlled ambients in a glovebox: pure N_2, O_2:N_2 = 1:4, and moisturized N_2 with ~50% relative humidity (details of controlled ambients described elsewhere[12]). The device was kept in each ambient overnight prior to the measurement. Transfer and output curves were swept both from negative to positive gate bias and in the opposite direction. No hysteresis was observed, and the drain current $I_d(V_{gs}, V_{ds})$ exhibited the same value at the same gate and drain biases V_{gs} and V_{ds} independent of the sweeping sequence, indicating true DC characteristics and accurate field effect mobility extraction.[12,13] Figure 2(a) shows the output characteristics with V_{ds} swept from 0 to +1 V and V_{gs} varied from –50 to +50 V in +10 V increments. Figure 2(b) plots two typical transfer curves, with V_{gs} swept from +50 to –50 V and from 0 to –100 V, respectively, and V_{ds} = +1 V in both sweeps. The gate leakage current was in the nA range for all measurements. Down to the most negative

gate bias available with the instrument (HP4145B), no channel conductance minimum was observed.

The electron field effect mobility μ is extracted as follows: The change in the sheet conductivity of graphene due to area carrier density modulation Δn is $\Delta\sigma = \Delta nq\mu$, where q is the elementary charge. The change in channel charge is $\Delta nq = C_i \Delta V_{gs}$, where C_i is the unit area gate capacitance. Obtaining $\Delta\sigma = (\Delta I_d/V_{ds})/(W/L)$ for ΔV_{gs} from the measured transfer characteristics, we calculate $\mu = \frac{(\Delta I_d / V_{ds})/(W/L)}{C_i \Delta V_{gs}}$. To determine the unit area gate capacitance, capacitors were built on the control substrate mentioned above by depositing Au top electrodes, and C_i was found to be 4.53 ± 0.05 nF/cm^2, corresponding to a 527 nm polystyrene thickness, consistent with ellipsometry measurement.[14] The extracted electron field effect mobility is 535 cm^2/Vs.

Our demonstration of the strong field effect was attributed to the patterned graphene active material and the gate-to-S/D overlaps among other factors, as compared to the previous attempt, where un-patterned graphene outside the channel region forms a parallel shunt conductance and the large gaps between the gate and S/D electrodes present significant series resistance, masking the channel conductance modulation.[4] Here, the graphene active layer is photolithographically patterned to eliminate the un-modulated parallel shunt conductance, taking advantage of the solvent compatibility of graphene. Overlaps between the gate and S/D [see Fig. 1(a)] are 125 μm each ensured by the mask layout, eliminating the un-modulated resistance in series with the channel.

Secondly, the fabrication process is designed to have minimum impact on the graphene. Graphene is known to be chemically robust, and very high mobility has been

demonstrated with lithographically patterned graphene. Nevertheless, several monolayers of graphene may be easily damaged by energetic particle bombardment. Therefore, we avoided dielectric deposition techniques that involve plasmas, and adopted a spin-coated polymer. Although spin coated polymer films are too thick for practical devices, this device configuration is sufficient for principle demonstration. Polystyrene was chosen because it is non-polar and therefore does not cause hysteresis in current-voltage measurements, ensuring accurate field effect mobility extraction.[12,13,15]

Although the field effect mobility achieved here is among the highest so far reported in epitaxial graphene,[16] it is more than one order of magnitude lower than measured in exfoliated graphene. This discrepancy is tentatively attributed to the rough morphology of the graphene layer, rather than being intrinsic to epitaxial graphene, since high Hall mobility has been measured by others in small patterned features of epitaxial graphene, although at cryogenic temperatures.[5] Here, we choose to use macroscopic device dimensions, not only for quick demonstration using existing masks, but more importantly to probe the average transport property over large area, relevant to wafer scale fabrication. The nominally on-axis (with small unintentional mis-orientation as used in this work) hexagonal SiC surface has random local undulations, resulting in steps with (0001) step surfaces and integer or half integer unit cell heights after H-etching.[11] More importantly, the subtractive thermal graphitization process on an oxidized substrate (due to air exposure prior to graphitization) causes the formation of more steps as shown in Fig. 1(c) as compared to Fig. 1(b), and the steps formed here can be deeper than a single unit-cell. All the step edges, pre-existing or formed during graphitization, will

cause current interruption (or scattering), lowering the extracted mobility. Future work will focus on the development of flatter graphitized surfaces.

Although it is not clear why no channel conductance minimum is observed in the available gate voltage range and only n channel FET behavior is obtained, the lack of p FET behavior is believed not to be inherent to epitaxial graphene but due to extrinsic doping. We consider doping caused by air exposure to be unlikely, however, since the device was thoroughly baked in N_2 prior to characterization and the measured characteristics are identical in various ambients. Prior to H-etching, the backside of the substrate was deposited with a Mo thin film, necessary for electron beam heating in the graphitization. Auger analysis revealed the presence of 0.10 monolayer of Mo in the near surface region of the graphene. It is likely that Mo acts as a donor, and at such a high doping level results in the lack of p channel behavior.

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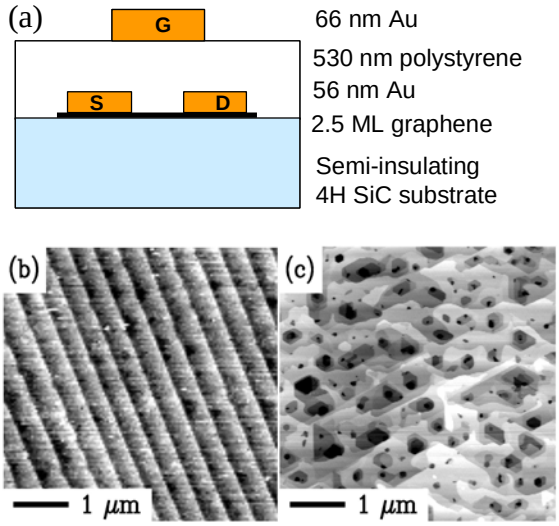
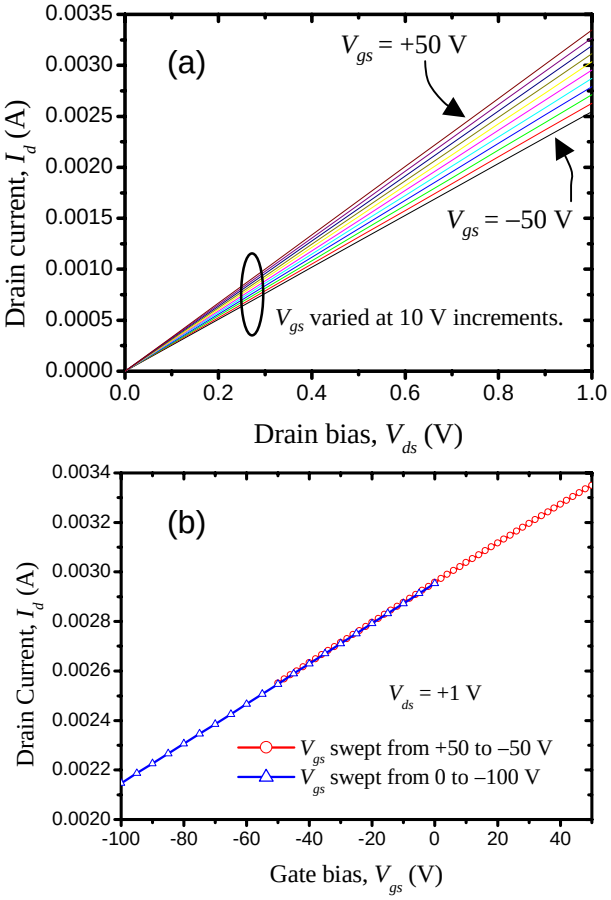
Figure captions

FIG. 1. (a) (Color online) Schematic cross-section of the semimetal graphene based transistor. (b) AFM image of the 4H SiC surface after H-etching prior to graphitization, displayed with gray scale range of 1.3 nm. (c) AFM image after graphitization, displayed with gray scale range of 3.1 nm.

FIG. 2. (Color online) Output (a) and transfer (b) characteristics of the semimetal graphene based transistor at room temperature. Results are identical for measurements of different voltage sweep sequences in various ambients. Gate leakage is in the nA range for all measurements. The extracted field effect mobility is 535 cm^2/Vs.


(a)
G
S
D
66 nm Au
530 nm polystyrene
56 nm Au
2.5 ML graphene
Semi-insulating
4H SiC substrate
(b)
1 μm
(c)
1 μm


(a)
V_{gs} = +50 V
V_{gs} = –50 V
V_{gs} varied at 10 V increments.
Drain current, I_d (A)
Drain bias, V_{ds} (V)
0.0035
0.0030
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
0.0
0.2
0.4
0.6
0.8
1.0
(b)
V_{ds} = +1 V
V_{gs} swept from +50 to –50 V
V_{gs} swept from 0 to –100 V
Drain Current, I_d (A)
Gate bias, V_{gs} (V)
0.0034
0.0032
0.0030
0.0028
0.0026
0.0024
0.0022
0.0020
-100
-80
-60
-40
-20
0
20
40